In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1-12. (Canceled)

13. (Currently Amended) A method for recovering a digital data signal (D_{out}) and a clock signal (Ck_{out}) comprising:

receiving a data signal (D_{in}) including a plurality of successive bits;

generating, from the data signal (D_{in}), the clock signal (Ck_{out}) with a resonator circuit;

delaying the data signal (D_{in}) to compensate for a delay created by the generating the clock signal (Ck_{out}) so that the data signal(D_{in}) is synchronized with the clock signal (Ck_{out});

phase locking the clock signal (Ck_{out}) to the delayed data signal by:

measuring, via a phase detector, a phase difference between the clock signal (Ck_{out}) and the delayed data signal ~~and by time delaying the clock signal (Ck_{out}) based on the phase difference~~, wherein measuring the phase difference includes sampling in the phase detector the delayed data signal with the clock signal (Ck_{out}) in three flip-flops at three different points in time; and

time delaying the clock signal (Ck_{out}) based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit;

sampling the delayed data signal at approximately the center of each bit with the delayed clock signal (Ck_{out}); and

generating, as a result of the sampling, the digital data signal (D_{out}).

14. (Canceled)

15. (Currently Amended) The method of claim 13 [[14]] further comprising:

generating a second steering signal based on the frequency difference between the clock signal (Ckout) and an output signal from the resonator circuit;

controlling, with the second steering signal, a controlled oscillator in a frequency locked loop; and

frequency locking the clock signal (Ckout) to the output of the resonator circuit.

16. (Previously Presented) The method of claim 15 further comprising:

filtering the first steering signal with a first low pass filter; and

filtering the second steering signal with a second low pass filter.

17. (Previously Presented) The method of claim 16 wherein a cut-off frequency of the first low pass filter is approximately 10 to 20 times smaller than the cut-off frequency of the second low pass filter.

18. (Previously Presented) The method of claim 16 wherein a cut-off frequency of the first low pass filter is between 1 KHz and 50 KHz and a cut-off frequency of the second low pass filter is between 40 KHz and 2 MHz.

19. (Previously Presented) The method of claim 13 wherein a data rate of the data signal (D_{in}) is 622 MHz, 2.5 GHz, or 10 GHz.

20. (Currently Amended) A circuit for recovering a digital data signal (Dout) and a clock signal (Ckout) from a received data signal (Din), the received data signal (Din) including a number of successive bits, the circuit comprising:

means for generating a clock signal from the received data signal (Din);

means for delaying the data signal (Din) by sampling the received data signal (Din) with the clock signal (Ckout) so that the delayed data signal is synchronized with the clock signal (Ck_{out});

means for measuring a phase difference between the clock signal (Ckout) and the delayed data signal and for phase locking the clock signal (Ckout) and the delayed data signal by time delaying the clock signal (Ckout) depending on the phase difference, wherein the means for measuring the phase difference measures the phase difference by sampling the delayed data signal with the clock signal (Ckout) in three flip-flops at three different points in time;

means for time delaying the clock signal (Ckout) based ~~depending~~ on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit;

means for sampling the delayed data signal at approximately the center of each bit according to the delayed clock signal (Ckout); and

means for generating, as a result of the sampling, the digital data signal (D_{out}).

21. (Canceled)

22. (Currently Amended) The circuit of claim 20 [[21]] further comprising:

a frequency locked loop to frequency lock the clock signal and an output of the resonator circuit, the frequency locked loop including a controlled oscillator, the controlled oscillator to respond to a second steering signal, wherein the second steering signal is based on a frequency difference between the clock signal (Ckout) and an output signal from the resonator circuit.

23. (Previously Presented) The circuit of claim 22 further comprising:

a first low pass filter to filter the first steering signal; and

a second low pass filter to filter the second steering signal.

24. (Previously Presented) The circuit of claim 23 wherein a cut-off frequency of the first low pass filter is approximately 10 to 20 times smaller than the cut-off frequency of the second low pass filter.

25. (Previously Presented) The circuit of claim 23 wherein a cut-off frequency of the first low pass filter is between 1 KHz and 50 KHz and a cut-off frequency of the second low pass filter is between 40 KHz and 2 MHz.

26. (Currently Amended) A circuit for recovering a digital data signal (Dout) and a clock signal (Ckout) from a received data signal (Din), the received data signal (Din) including a number of successive bits, the circuit comprising:

a resonator circuit to generate a clock signal from the received data signal (Din);

a delay element to delay the received data signal (Din) by sampling the received data signal (Din) with the clock signal (Ckout) so that the delayed data signal is synchronized with the clock signal (Ck_{out});

a phase detector to measure a phase difference between the clock signal (Ckout) and the delayed data signal and for phase locking the clock signal (Ckout) and the delayed data signal by time delaying the clock signal (Ckout) depending on the phase difference, wherein measuring the phase difference includes sampling the delayed data signal with the clock signal (Ckout) in three flip-flops at three different points in time;

a controllable delay unit to delay the clock signal (Ckout) ~~depending~~ based on the phase difference by generating a first steering signal based on the phase difference and controlling, with the first steering signal, a controlled delay unit;

a flip-flop to sample the delayed data signal at approximately the center of each bit according to the delayed clock signal (Ckout); and

a data buffer to generate, as a result of the sampling, the digital data signal (D_{out}).

27. (Canceled)

28. (Currently Amended) The circuit of claim 26 [[27]] further comprising:

a frequency locked loop to frequency lock the clock signal and an output of the resonator circuit, the frequency locked loop including a controlled oscillator, the controlled oscillator to respond to a second steering signal, wherein the second steering signal is based on a frequency difference between the clock signal (Ckout) and an output signal from the resonator circuit.

29. (Previously Presented) The circuit of claim 28 further comprising:

a first low pass filter to filter the first steering signal; and

a second low pass filter to filter the second steering signal.

30. (Previously Presented) The circuit of claim 29 wherein a cut-off frequency of the first low pass filter is approximately 10 to 20 times smaller than the cut-off frequency of the second low pass filter.

31. (Previously Presented) The circuit of claim 29 wherein a cut-off frequency of the first low pass filter is between 1 KHz and 50 KHz and a cut-off frequency of the second low pass filter is between 40 KHz and 2 MHz.